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EXAMINER	
TRINH, MICHAEL MANH	

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2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,457	DONG, CHA DEOK	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006 and 13 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment and RCE filed on February 21, 2006. Claims 1-14 are pending.

Claim Rejections - 35 USC § 112

1. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re base claims 1 and 6: the original specification does not support and describe the claimed limitations of "performing a second ion implantation into a **whole** active region (Fig. 5, A) to compensate for an ion concentration..." (Bold added).

Applicant remarked (1/13/06 remark page 7) that "...the invention provides a step of performing a second ion implantation into a whole active region (Fig.5, A) to compensate for an ion concentration of the active region (Fig. 5, A)" and "...the second ion of the present invention is implanted through a gate oxide film, a polysilicon film and a pad nitride film, on the other hand, the ion of Wu is implanted through laminated oxide film...". However, nowhere in the original specification mention and provide a support for "second ion implantation into a whole active region (Fig. 5, A". Nowhere in the original specification provides a support for second ion implanting through a gate oxide film, a polysilicon film, and a pad nitride film. To the contrary, the combined thick thickness of the layers of pad nitride 16, polysilicon 14, and gate oxide 12 formed on the whole active region A, as shown in Figures 4-5, would effectively act as a barrier mask to prevent the whole active region A from being implanted with the second ions at such a low energy band of 10 to 25 Kev, wholly and entirely into the active region A (see Figs 4-5, specification paragraph 0025, and claim 6).

(Dependent claims are rejected as depending on rejected base claims).

Claim Rejections - 35 USC § 102

2. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (2002/0115270).

Wu teaches a method for forming a device isolation film in a semiconductor device, comprising the steps of: performing a first ion implantation 102 for controlling a threshold voltage on a surface of a semiconductor substrate 100 (Fig 3A, paragraph 0014); forming a trench having sidewall to define an active region and a device isolation region by etching a portion of the semiconductor substrate of a device isolation region (Figs 3B-3C; paragraph 0016); forming a side wall oxidation film 105 at the side wall of the trench by performing an oxidation process (Fig 3D; paragraph 0016); performing a second ion implantation 102b into a whole active region at the trench sidewall surface to compensate for an ion concentration of the active region (Fig 3D; paragraph 0016); and forming a device isolation film 106 by burying the oxidation film inside the trench (Figs 3E-3F, paragraph 0017; Figs 4A-4F, paragraphs 0020-0021). Re claim 5, wherein boron is used as an ion for implanting to control the threshold voltage (paragraph 0014).

Claim Rejections - 35 USC § 103

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) taken with Oda et al (2002/0086498).

Wu teaches a method for forming a device isolation film in a semiconductor device, as applied to claim 1 above.

Re claim 2, Wu already teaches performing an oxidation to form the sidewall oxidation film 105 having a thickness in a range of 50 to 150 Angstroms. Wu does not mention the oxidation to round an upper portion or bottom corner of the trench.

However, Oda et al teach (at Figs 2, paragraph 0045; Figs 3-9; paragraphs 0046-0052) when forming the trench, the side wall oxidation film 5 formed by oxidation to perform a rounding treatment to round on an upper corner portion of the trench, and to suppress fluctuation of a threshold voltage in an upper corner portion of the trench isolation (paragraphs 0017-0021), wherein bottom corners of the trench is inherently rounded during the same oxidation step, and

wherein an adhesive strength of the oxidation film to be buried inside the trench is also inherently increased due to the formation of the sidewall oxidation film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device isolation film in a semiconductor device of Wu by rounding the upper portion or corners of the trench at the same time during the oxidation step to the sidewall oxidation film as taught by Oda. This is at least because of the desirability to suppress fluctuation of a threshold voltage in an upper corner portion of the trench isolation. Also, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of thickness in a range of 50 to 150 Angstroms, as disclosed by Wu, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) taken with Hong (6,030,882).

Wu teaches a method for forming a device isolation film in a semiconductor device, as applied to claim 1 above.

Re claim 3, Wu already teaches performing an oxidation to form the sidewall oxidation film, but lacks mentioning by a dry oxidation at a temperature of 800-900°C.

However, Hong teaches (at Figs 2C-2D; col 4, lines 13-25) forming a sidewall oxidation film 218 on sidewalls of the trench by dry oxidation at a temperature of about 900°C.

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of temperature of about 900°C in the dry oxidation to form the sidewall oxidation film on sidewalls of the trench, as disclosed by Hong, which temperature is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the

best results, wherein the implanted ions are prohibiting from diffusion at that temperature, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation", *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934); wherein the dry oxidation is effectively process for forming a thin uniform sidewall oxidation film on the sidewalls of the trench as a liner oxide layer.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) taken with Oda et al (2002/0086498).

Wu teaches a method for forming a device isolation film in a semiconductor device, as applied to claim 1 above.

Re claims 4-5, Wu already teaches performing an ion implantation process on an active region after the oxidation process, but lack mentioning the implantation at a dose of 1E 11 to 1E12 ion/cm^2 in an energy band of 10 Kev to 25 Kev.

However, Oda teaches performing an ion implantation process on an active region after the oxidation process, wherein the implantation is performed at a dose of 5E 11 to 1E14 ion/cm^2 in an energy band of 10 Kev to 30 Kev.

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to perform the ion implantation of Wu by selecting the portion of the prior art's range of dose and energy, as disclosed by Oda, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

6. Claims 6,14 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu (2002/0115270) taken with Sung (5,550,078).

Wu teaches a method for forming a device isolation film in a semiconductor device, comprising the steps of: performing a first ion implantation (102 in Fig 3A; 200 in Fig 4A) for controlling a threshold voltage on a surface of a semiconductor substrate 100 (Fig 3A, paragraph 0014; Fig 4A, paragraph 0020); sequentially forming a gate oxide film 201, a polysilicon film 202, and a pad nitride 203 on the semiconductor substrate 100 (Fig 4A; paragraphs 0020); forming a trench having sidewall to define an active region and a device isolation region by etching a portion of the semiconductor substrate of a device isolation region (Figs 3B-3C; paragraph 0016; Fig 3D; paragraph 0020); forming a side wall oxidation film (105 in Fig 3D; 205 in Fig 4D) at the side wall of the trench by performing an oxidation process (Fig 3D; paragraph 0016; Figs 4D-4F; paragraphs 20-21); performing a second ion implantation (102b in Fig 3D; 200b in Fig 4D) into a whole active region at the trench sidewall surface to compensate for an ion concentration of the active region (Fig 3D; paragraph 0016; Fig 4D); removing the pad nitride 203a (paragraph 0022); and forming a device isolation film (106 in Fig 3E; 206 in Fig 4E) by burying the oxidation film inside the trench (Figs 3E-3F, paragraph 0017; Figs 4A-4F, paragraphs 0020-0021). Re claim 14, wherein boron is used as an ion for implanting to control the threshold voltage (paragraphs 0014 and 20).

Wu teaches ion implanting to form threshold voltage (Fig 4A), but does not clearly mention forming a screen oxide film before implantation and removing it thereafter.

However, Sung teaches (at Figs 4-6; col 5, line 55-67; col 6) forming a screen oxide film 9 to protect the semiconductor substrate (Fig 5); performing an ion implantation for controlling a threshold voltage 10; and removing the screen oxide film 9 thereafter.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform an ion implantation for controlling a threshold voltage of Wu by forming a screen oxide film before ion implantation and removing it thereafter, as taught by Sung. This is because of the desirability to protect the semiconductor substrate from damaging due to the ion implantation.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Sung (5,550,078), as applied to claim 6 above, taken with Oda et al (2002/0086498).

Wu and Sung teach a method for forming a device isolation film in a semiconductor device, as applied to claim 6 above.

Re claim 11, Wu already teaches performing an oxidation to form the sidewall oxidation film 105 having a thickness in a range of 50 to 150 Angstroms. Wu does not mention the oxidation to round an upper portion or bottom corner of the trench.

However, Oda et al teach (at Figs 2, paragraph 0045; Figs 3-9; paragraphs 0046-0052) when forming the trench, the side wall oxidation film 5 formed by oxidation to perform a rounding treatment to round on an upper corner portion of the trench, and to suppress fluctuation of a threshold voltage in an upper corner portion of the trench isolation (paragraphs 0017-0021), wherein bottom corners of the trench is inherently rounded during the same oxidation step, and wherein an adhesive strength of the oxidation film to be buried inside the trench is also inherently increased due to the formation of the sidewall oxidation film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device isolation film in a semiconductor device of Wu by rounding the upper portion or corners of the trench at the same time during the oxidation step to the sidewall oxidation film as taught by Oda. This is at least because of the desirability to suppress fluctuation of a threshold voltage in an upper corner portion of the trench isolation. Also, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of thickness in a range of 50 to 150 Angstroms, as disclosed by Wu, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Sung (5,550,078), as applied to claim 6 above, taken with Hong (6,030,882).

Wu and Sung teach a method for forming a device isolation film in a semiconductor device, as applied to claim 6 above.

Re claim 12, Wu already teaches performing an oxidation to form the sidewall oxidation film, but lacks mentioning by a dry oxidation at a temperature of 800-900°C.

However, Hong teaches (at Figs 2C-2D; col 4, lines 13-25) forming a sidewall oxidation film 218 on sidewalls of the trench by dry oxidation at a temperature of about 900°C.

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to select the portion of the prior art's range of temperature of about 900°C in the dry oxidation to form the sidewall oxidation film on sidewalls of the trench, as disclosed by Hong, which temperature is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, wherein the implanted ions are prohibiting from diffusion at that temperature, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation", *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934); wherein the dry oxidation is effectively process for forming a thin uniform sidewall oxidation film on the sidewalls of the trench as a liner oxide layer.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Sung (5,550,078), as applied to claim 6 above, taken with Oda et al (2002/0086498).

Wu and Sung teach a method for forming a device isolation film in a semiconductor device, as applied to claim 6 above.

Re claim 13, Wu already teaches performing an ion implantation process on an active region after the oxidation process, but lack mentioning the implantation at a dose of 1E 11 to 1E12 ion/cm^2 in an energy band of 10 Kev to 25 Kev.

However, Oda teaches performing an ion implantation process on an active region after the oxidation process, wherein the implantation is performed at a dose of 5E 11 to 1E14 ion/cm^2 in an energy band of 10 Kev to 30 Kev.

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to perform the ion implantation of Wu by selecting the portion of the prior art's range of dose and energy, as disclosed by Oda, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

10. Claims 7,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Sung (5,550,078), as applied to claim 6 above, and further of Houlihan (2001/0021545) or Dong (2003/0119256).

The references including Wu and Sung teach a method for forming a device isolation film in a semiconductor device, as applied to claim 6 above.

Re claims 7, the references teach forming the screen oxide, but lack mentioning thickness of about 50-70 Angstroms by wet or dry oxidation at 700-900° C. Re claim 10, Wu already teaches forming the pad nitride film 203 by low pressure chemical vapor deposition, but lack mentioning a thickness of about 900-2000Angstroms.

However, re claim 7, Sung already teaches forming a screen oxide film 9 having a thickness of about 150-250 Angstroms by thermal oxidation at 850-950° C (col 4, lines 55-65). Houlihan teaches (at col 4, lines 63-67) forming a screen oxide film 24 having a thickness of about 50-100 Angstroms. Re claim 10, Houlihan also teaches forming the pad nitride film 27 having a thickness of about 800-1000Angstroms (col 5, lines 12-15). Dong also teaches (at paragraph 25) forming a screen oxide film 26 having a thickness of about 50-70 Angstroms by wet or dry oxidation at 700-900 °C (re claim 7), wherein a pad nitride 16 is formed by LPCVD (paragraph 13, re claim 10).

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to perform the screen oxide film and the pad nitride film of the references including Wu by selecting the portion of the prior art's range of

thickness and temperature, as disclosed by Sung and Houlihan or Dong, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Sung (5,550,078), as applied to claim 6 above, and further of Kim (2003/0067050) and/or Dong (2003/0119256).

The references including Wu and Sung teach a method for forming a device isolation film in a semiconductor device, as applied to claim 6 above.

Re claim 8, the references including Wu teach forming the gate oxidation film, but lack detailing about thickness, annealing time and temperature.

However, Sung teaches forming a gate oxidation film by thermal grown at a temperature of about 850-950°C to a thickness up to 200 Angstroms (col 5, lines 8-12). Kim teaches (at paragraph 24) forming a high voltage gate oxide film having a thickness of 300-1000 Angstroms. Dong teaches (at paragraph 27) forming a tunnel gate oxide film 28 by wet oxidation at 750-800°C and nitrogen annealing at a temperature of 900-910°C for 20-30 minutes.

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to perform the gate oxide film of the references including Wu by selecting the portion of the prior art's range of thickness and temperature, as disclosed by Sung and Kim and/or Dong, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, to form a high voltage transistor, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (2002/0115270) and Sung (5,550,078), as applied to claim 6 above, and further of Sung et al (6,180,453) and/or Dong (2003/0119256).

The references including Wu and Sung teach a method for forming a device isolation film in a semiconductor device, as applied to claim 6 above.

Re claim 9, the references including Wu teach forming the polysilicon film 202, but lack detailing about thickness, gases, pressure, and temperature as recited in claim 9.

However, Sung '078 teaches (col 5, lines 12-15) forming a polysilicon film 14 by LPCVD at a temperature of about 550-650° C using PH_3 gas and a silicon source gas, to a thickness of about 1000-4000 Angstroms. Sung et al '453 teaches (at col 3, lines 59-65) forming a polysilicon film 6 by LPCVD using PH_3 gas and a silane source gas, to a thickness of about 500-1000 Angstroms. Dong teaches (at paragraph 35-36) forming a polysilicon film by LPCVD at a temperature of about 510-550° C using PH_3 gas and a SiH_4 or Si_2H_6 source gas, to a thickness of about 500-1000 Angstroms, at pressure of 0.1 to 0.3 Torr.

Therefore, the subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to perform the polysilicon film of the references including Wu by selecting the portion of the prior art's range of thickness, pressure, temperature, gases, as disclosed by Sung '078 and Sung et al '453, and/or Dong, which is within the range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

Response to Amendment

13. Applicant's remarks submitted January 13, 2006 have been fully considered but they are not persuasive and in moot in view of the new ground(s) of rejection.

Applicant remarked (1/13/06 remark page 7) that "...the invention provides a step of performing a second ion implantation into a whole active region (Fig.5, A) to compensate for an ion concentration of the active region (Fig. 5, A)" and "...the second ion of the present invention is implanted through a gate oxide film, a polysilicon film and a pad nitride film, on the other hand, the ion of Wu is implanted through laminated oxide film...". However, nowhere in the original specification mention and provide a support for "second ion implantation into a whole active region (Fig. 5, A". Nowhere in the original specification provides a support for second ion implanting through a gate oxide film, a polysilicon film, and a pad nitride film.

To the contrary, the combined thick thickness of the layers of pad nitride 16, polysilicon 14, and gate oxide 12 formed on the whole active region A, as shown in Figures 4-5, would effectively act as a barrier mask to prevent the whole active region A from being implanted with the second ions at such a low energy band of 10 to 25 Kev, wholly and entirely into the active region A (see Figs 4-5, specification paragraph 0025, and claim 6).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-15

Michael Trinh
Primary Examiner